AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings of claims for this application:

Listing of Claims:

1. (Currently amended) An apparatus comprising:

groups of image sensors, each group comprising subgroups of sensors;

subgroup select circuits, each of which is coupled to an output from a respective subgroup of sensors;

group select circuits, each of which is coupled to outputs from subgroup select circuits associated with a respective one of the groups;

a first bus for each group coupled to the outputs of the associated subgroup select circuits;

a common output bus for receiving signals from each of the groups, the common output bus connected to a readout circuit, the readout circuit responsive to a sensed charge;

a controller for providing control signals to the subgroup select circuits and the group select circuits to selectively enable the respective subgroup select circuits and group select circuits to pass signals from the sensors to a readout circuit one sensor at a time; and

a first isolation circuit coupled to each first bus for selectively isolating each group from the readout circuit, the first isolation circuit comprising a switch for selectively connecting the first bus to a predetermined voltage.

2. (Original) The apparatus of claim 1 wherein the sensors comprise active pixel sensors.

3. (Previously presented) The apparatus of claim 1 further comprising a second bus coupled to the outputs of the group select circuits and the readout circuit.

4. (Original) The apparatus of claim 1 wherein the number of group select circuits is approximately equal to the square root of the number of subgroup select circuits.

5. (Original) The apparatus of claim 1 wherein a ratio of the number of subgroup select circuits to group select circuits is in a range of 10:1 and 40:1.

6. (Original) The apparatus of claim 5 wherein the ratio is in a range of 15:1 and 30:1.

7. (Previously presented) The apparatus of claim 1 wherein each group select circuit comprises a transistor switch with a respective gate terminal for receiving a control signal from the controller, wherein when the switch is turned on, the group select circuit is enabled to pass signals from associated subgroup select circuits to the first bus, and when the switch is turned off, the group select circuit is disabled from passing signals from the associated subgroup select circuits to the first bus.

8. (Previously presented) The apparatus of claim 7 wherein each subgroup select circuit comprises a transistor switch with a respective gate terminal for receiving a control signal from the controller, wherein when the subgroup select circuit switch is turned on, the subgroup select circuit is enabled to pass signals from an associated subgroup of sensors, and when the subgroup select circuit switch is turned off, the subgroup select circuit is disabled from passing signals from the associated subgroup of sensors to the first bus.

9. (Original) The apparatus of claim 8 wherein the controller is configured for generating the control signals to enable and disable the group select circuit switches and the subgroup select circuit switches in a predetermined sequence.

10. (Previously presented) The apparatus of claim 9 wherein the controller is configured to provide the control signals to enable the switches in the group select circuits sequentially, and, while a particular group select switch is enabled, to enable the subgroup select circuits associated with the particular group select circuit sequentially, one at a time.

11. (Previously presented) The apparatus of claim 1 wherein the controller is configured to enable and subsequently disable each group select circuit, one at a time, in a sequential manner.

12. (Original) The apparatus of claim 1 wherein each group select circuit comprises a pair of NMOS transistor switches.

13. (Previously presented) The apparatus of claim 3 comprising:

supergroups of sensors;

supergroup select circuits, each of which is coupled to outputs from group select circuits associated with a respective one of the supergroups; and

a second isolation circuit coupled to each second bus for selectively isolating each supergroup from the readout circuit, the second isolation circuit comprising a switch for selectively connecting the first bus to a predetermined voltage,

wherein the controller is configured to provide control signals to the supergroup select circuits to selectively enable a supergroup select circuit to pass a signal from the second bus to a third, common output bus.

14. (Original) The apparatus of claim 13 wherein an output of each supergroup select circuit is coupled electrically to a common output bus.

15. (Original) The apparatus of claim 13 wherein each supergroup select circuit comprises a transistor switch with a respective gate terminal for receiving a control signal from the controller.

16. (Previously presented) A method comprising:

(a) selectively enabling a group select circuit to electrically couple a charge mode read-out amplifier to a respective set of subgroup select circuits;

(b) when the group select circuit is enabled, enabling a un-amplified pixel output signal to pass from each subgroup select circuit of the respective set of subgroup select circuits in a sequential manner through the group select circuit to the charge mode read-out amplifier; and

(c) subsequently disabling the group select circuit to electrically isolate the charge mode read-out amplifier from the respective set of subgroup select circuits.

17. (Original) The method of claim 16 further comprising repeating (a), (b) and (c) with respect to another group select circuit and respective set of subgroup select circuits.

18. (Previously presented) The method of claim 16 wherein disabling the group select circuit occurs after a un-amplified pixel output signal has passed from each subgroup select circuit in the respective set of subgroup select circuits through the group select circuit to the charge mode read-out amplifier.

19. (Previously presented) A method comprising:

(a) selectively enabling a supergroup select circuit from a set of supergroup select circuits and a series-connected group select circuit from an associated set of group select circuits to electrically couple a charge mode read-out amplifier to a respective set of subgroup select circuits;

(b) when the series-connected group select circuit and supergroup select circuit are so enabled, enabling a un-amplified pixel output signal to pass from each subgroup select circuit of the respective set of subgroup select circuits in a sequential manner through

the series-connected group select circuit and supergroup select circuit to the charge mode read-out amplifier; and

(c) disabling the group select circuit to electrically isolate the charge mode read-out amplifier from the respective set of subgroup select circuits.

20. (Original) The method of claim 19 further comprising repeating (a), (b) and (c) with respect to another series-connected group select circuit associated with the supergroup select circuit and a respective set of subgroup select circuits.

21. (Previously presented) The method of claim 19 wherein disabling the group select circuit occurs after a un-amplified pixel output signal has passed from each subgroup select circuit in the respective set of subgroup select circuits through the group select circuit and to the charge mode read-out amplifier.

22. (Original) The method of claim 19 further comprising disabling the supergroup select circuit to electrically isolate the charge mode read-out amplifier from the respective set of group select circuits and subgroup select circuits.

23. (Original) The method of claim 22 wherein disabling the supergroup select circuit occurs after a pixel output signal has passed from each subgroup select circuit in the respective sets of subgroup select circuits associated with each of the group select circuits through the supergroup select circuit and to the charge mode read-out amplifier.

Claim 24 (Canceled).

25. (Currently amended) A method of obtaining a readout of a pixel sensor array comprising:

organizing pixel sensors of an array into groups comprising a plurality of subgroups of sensors, the outputs of each subgroup coupled to an associated subgroup select circuit and the outputs of each subgroup select circuit coupled to an associated group select circuit;

selectively enabling a group select circuit and a subgroup select circuit to allow ~~sequential readout~~ a signal from each sensor in said subgroup to pass sequentially to a readout circuit electrically connected to said group select circuit;

sensing a charge at the readout circuit; and

selectively isolating from said readout circuit the groups of pixels not associated with the selectively enabled group select circuit by disabling the subgroup select circuits and group select circuits not associated with the selectively enabled group select circuit and applying a predetermined voltage to at least one first bus coupled to the disabled group select circuits by operating a switch coupled to the at least one first bus.

Claims 26-27 (Canceled).

28. (Previously presented) The method of claim 25 further comprising the step of organizing groups of subgroups of said sensors into supergroups, wherein the outputs of group select circuits associated with a supergroup are connected to a respective supergroup select circuit.

29. (Previously presented) The method of claim 28 further comprising the step of coupling each supergroup select circuit to an associated second bus, wherein the readout signals from each sensor in said supergroup will travel through said second bus.

30. (Previously presented) The method of claim 29 further comprising the step of selectively applying the predetermined voltage at each second bus.

31. (Currently amended) An imager device comprising:

groups of image sensors, each group comprising a plurality of columns of an image sensor array;

a plurality of column select circuits, each of which is coupled to an output from a column of sensors;

a plurality of group select circuits, each of which is coupled via a first bus to outputs from the column select circuits associated with a respective one of the groups;

a readout circuit connected to outputs of said group select circuits, the readout circuit comprising a charge mode amplifier; and

a controller for providing control signals to the column select circuits and the group select circuits to selectively enable the respective column select circuits and group select circuits to pass signals from the sensors to said readout circuit one sensor at a time; ~~and~~

~~a first isolation circuit coupled to each first bus for selectively isolating each group from the readout circuit, the first isolation circuit comprising a switch for selectively connecting the first bus to a predetermined voltage~~.

32. (Previously presented) The imager device of claim 31 wherein the sensors comprise active pixel sensors.

Claim 33 (Canceled).

34. (Currently amended) An imager device comprising:

an array of image sensors organized into supergroups comprising groups of subgroups of image sensors;

subgroup select circuits, each of which is coupled to outputs of the sensors of a respective subgroup;

group select circuits, each of which is coupled to outputs of subgroup select circuits associated with a respective one of the groups;

supergroup select circuits, each of which is coupled to outputs of group select circuits associated with a respective one of the supergroups;

at least two group buses, each group bus coupled to outputs of the subgroup select circuits associated with a respective group;

a common output bus coupled to outputs of the group select circuits and to a readout circuit, the readout circuit configured to amplify signals received from the image sensors; and

a controller for providing control signals to the image sensors to produce a readout signal and to the supergroup select circuits, group select circuits, and subgroup select circuits to selectively enable the respective supergroup, group, and subgroup select circuits to pass output signals from the image sensors to the readout circuit one sensor at a time~~; and~~

~~a first isolation circuit coupled to each group bus for selectively isolating each group from the readout circuit, the first isolation circuit comprising a switch for selectively connecting the first bus to a predetermined voltage~~.

35. (Previously presented) The apparatus of claim 1, wherein the predetermined voltage is one of a supply voltage for the apparatus or a ground potential.

36. (Previously presented) The method of claim 25, wherein the predetermined voltage is one of a supply voltage for the array or a ground potential.

37. (New) The apparatus of claim 1, wherein the common output bus is connected between outputs from the group select circuits and the readout circuit.

38. (New) The apparatus of claim 13, wherein the common output bus is connected between outputs from the supergroup select circuits and the readout circuit.

39. (New) An apparatus comprising:

groups of image sensors, each group comprising subgroups of sensors;

subgroup select circuits, each of which is coupled to an output from a respective subgroup of sensors;

group select circuits, each of which is coupled to outputs from subgroup select circuits associated with a respective one of the groups;

a first bus for each group coupled to the outputs of the associated subgroup select circuits; and

a controller for providing control signals to the subgroup select circuits and the group select circuits to selectively enable the respective subgroup select circuits and group select circuits to pass signals from the sensors to a readout circuit one sensor at a time, the readout circuit responsive to a sensed charge.